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EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/841,569	ECKELMAN ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's arguments/amendments with respect to amended claims 1 and previously submitted claims 2-7 filed July 29, 2005 have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, "...the references do not teach handling multiple bit failure detection..." Examiner respectfully disagrees. Yasui teaches (abstract) a method of analyzing a repair of failure memory cell in a memory is provided, which is **capable of searching a must-repair of a memory at high speed** and of performing a simulation process for relieving a must-repair at high speed at the time point when it has been detected. There are provided **a row address failure number counter/memory for counting the number of failure memory cells on each row address in the row address direction and storing it and a column address failure number counter/memory for counting the number of failure memory cells on each column address in the column address direction** and storing it. The Examiner would like to point out that the failure number counter taught by Yasui clearly shows that multiple bit errors/failures are detected for the row and column. The stored value in either one counter/memory is read out and the number of failure memory cells on each address is compared with the number of spare lines. The state that the number of failure memory cells on each address is greater than the number of spare lines is determined to be a must-repair, and a simulation process for relieving the failure is executed at the time point when the must-repair has been detected.

Applicant contends, "...the references cited by the examiner are external to the chip being tested..." Examiner is not sure about this contention. However, it is believed that Applicants intended to say the references do not teach how to implement on chip testing at any level. The Examiner would like to point out that the claim suggests that the assembly test may be selected from any of the given levels. Surely, the references teach at least one if not all the possible level. Furthermore, these various levels of tests are well known in the art and cannot render the claims patentably distinct or non-obvious. Similar reasoning applies for on chip testing. See *In re Larson 144 USPQ 347 (CCPA 1965).*

Applicant contends, "...the prior arts of record do not show the skipping process for reuse of chip circuitry..." The Examiner respectfully disagrees. Yasui teaches (Figure 5) a block diagram showing a schematic configuration of an example of a memory testing apparatus having a conventional failure relief analyzer. This memory testing apparatus TES comprises, roughly speaking, a main controller 111, a pattern generator 112, a timing generator 113, a waveform formatter 114, a logical comparator 115, a driver 116, an analog level comparator (hereinafter referred to as a comparator) 117, a failure analysis memory 118, a failure relief analyzer 120, a logical amplitude reference voltage source 121, a comparison reference voltage source 122 and a device power source 123. **The main controller 111 is generally constituted by a computer system in which a test program PM created by a user (programmer) is loaded in advance, and the control of the entire memory testing apparatus is performed in accordance with the test program PM.** This main controller 111 is connected, via a tester bus BUS, to the pattern generator 112, the timing generator 113, the failure analysis memory 118, the failure relief analyzer 120 and the like. Although not shown, the logical amplitude reference voltage source

121, the comparison reference voltage source 122 and the device power source 123 are also connected to the main controller 111. Furthermore, the Examiner would like to point out that Yasui teaches the main controller 111 is constituted by a computer system in which a test program PM created by a user (programmer) is loaded in advance, and the control of the entire memory testing apparatus is performed in accordance with the test program PM and therefore could very well be preset to skipping to a programmed amount as stated in the present application. Sato teaches (Figure 16) each of the memory controllers comprises a refresh timer for generating a refresh request signal, a failure storage trigger generator for being supplied with the failure storage signal and a one-address storage signal which is outputted each time the storage of failure data into the corresponding DRAM is finished, turning on a failure storage operation flag and outputting a failure storage trigger signal to start storing the failure data from the buffer memory means into the DRAM when a refresh operation flag is turned off and a count of the failure storage signal and a count of the one-address storage signal disagree with each other, a refresh trigger generator responsive to the refresh request signal for turning on the refresh operation flag and outputting a refresh start signal when the failure storage operation flag is turned off, a read/modify/write circuit for effecting the read/modify/write mode to store failure data into the DRAM, a timing generation memory for storing in advance timing data to refresh the DRAM and store the failure data into the DRAM, a program counter for generating address pointers for the timing generation memory, a sequence memory for storing sequence data to increment, decrement, and hold data in the program counter, the sequence memory having address pointers generated by the program counters, and a sequence controller for operating the program counter according to the sequence data outputted from the sequence memory in

response to the failure storage trigger signal outputted from the failure storage trigger generator or the refresh start signal outputted from the refresh trigger generator. The failure storage trigger generator comprises an buffer memory storage counter for counting the failure storage signal, a DRAM storage counter for counting the one-address storage signal, a counter comparator for comparing a count of the buffer memory storage counter and a count of the DRAM storage counter with each other, and a circuit for generating and outputting the failure storage trigger signal when the counts of the buffer memory storage counter and the DRAM storage counter disagree with each other and failure data is not stored into the DRAM, and when the counts of the buffer memory storage counter and the DRAM storage counter disagree with each other and the page mode or the read/modify/write mode for storing failure data into the DRAM is finished. Each of the memory controllers comprises a refresh timer for generating a refresh request signal, a read/write trigger generator for being supplied with the failure storage signal and a one-address storage signal which is outputted each time the storage of failure data into the corresponding DRAM is finished, turning on a read/write operation flag and outputting a read/write trigger signal to start a read/write mode of operation of the DRAM when a refresh operation flag is turned off and the read/write request signal is supplied, a refresh trigger generator responsive to the refresh request signal for turning on the refresh operation flag and outputting a refresh start signal when the failure storage operation flag is turned off, a circuit for effecting operation modes of the DRAM, a timing generation memory for storing in advance timing data to refresh the DRAM and store the failure data into the DRAM, a program counter for generating address pointers for the timing generation memory, a sequence memory for storing sequence data to increment, decrement, and hold data in the program counter, the sequence memory having

address pointers generated by the program counters, an operation mode register for storing start addresses of the timing generation memory and the sequence memory in each of the operation modes, and a sequence controller for operating the program counter according to the sequence data outputted from the sequence memory in response to the read/write trigger signal outputted from the read/write trigger generator or the refresh start signal outputted from the refresh trigger generator.

The Examiner disagrees with the Applicant and maintains rejections with respect to amended claim 1 and previously presented claims 2-7. All arguments have been considered. It is the Examiner's conclusion that amended claims 1 and previously presented claims 2-7 are not patentably distinct or non-obvious over the prior art of record. See office action:

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasui (USPN 6594788B1) further in view of Sato (USPN 5790559).

As per claim 1, Yasui substantially teaches (title and abstract) a method of analyzing a repair of failure memory cell in a memory, which is capable of searching a must-repair of a memory at high speed and of performing a simulation process for relieving a must-repair at high speed at the time point when it has been detected. There are provided a row address failure number counter/memory for counting the number of failure memory cells on each row address in the row address direction and storing it and a column address failure number counter/memory for counting the number of failure memory cells on each column address in the column address direction and storing it. The stored value in either one counter/memory is read out and the number of failure memory cells on each address is compared with the number of spare lines. The state that the number of failure memory cells on each address is greater than the number of spare lines is determined to be a must-repair, and a simulation process for relieving the failure is executed at the time point when the must-repair has been detected. Furthermore, Yasui teaches (Figure 5) a block diagram showing a schematic configuration of memory testing apparatus having failure relief analyzer. This memory testing apparatus TES comprises a main controller 111, a pattern generator 112, a timing generator 113, a waveform formatter 114, a logical comparator 115, a driver 116, an analog level comparator 117, a failure analysis memory 118, a failure relief analyzer 120, a logical amplitude reference voltage source 121, a comparison reference voltage source 122 and a device power source 123. The main controller 111 is generally constituted by a computer system in which a test program PM created by a user (programmer) is loaded in advance, and the control of the entire memory testing apparatus is performed in accordance with the test program PM. This main controller 111 is connected, via a tester bus BUS, to the pattern generator 112, the timing generator 113, the failure analysis

memory 118, the failure relief analyzer 120 and the like. The logical amplitude reference voltage source 121, the comparison reference voltage source 122 and the device power source 123 are also connected to the main controller 111. Yasui teaches that before starting the test of the IC memory, various kinds of data are set by the main controller 111. After the various kinds of data have been set, the test of the IC memory is started. When the main controller 111 issues a test starting command to the pattern generator 112, the pattern generator 112 starts to generate a pattern. The pattern generator 112 supplies a test pattern data to the waveform formatter 114 in accordance with the test program PM. On the other hand, the timing generator 113 generates a timing signal (clock pulses) for controlling operation timings of the waveform formatter 114, the logical comparator 115 and the like.

Yasui does not explicitly teach, "...skip up to an 'Nth' failing cell and recording the failure of the subsequent 'Nth + 1' fail."

However, Sato, in an analogous art, teaches (abstract) a memory unit for storing failure data of a semiconductor memory under test comprises a plurality of interleaved DRAMs. A buffer memory temporarily stores failure data to be stored into the DRAMs and addresses thereof. The DRAMs are associated respectively with storage controllers which store failure addresses whose row addresses correspond to the DRAMs, among inputted failure addresses, into buffer memories associated respectively with the DRAMs. Write controllers are associated respectively with the DRAMs, for reading the failure data from the buffer memories and writing the failure data into the DRAMs in a high-speed write mode. In particular, Sato teaches (col. 8-9, lines 42-68 and 1-19) each of the memory controllers comprise a refresh timer for generating a refresh request signal, a read/write trigger generator for being supplied with the failure storage

signal and a one-address storage signal which is outputted each time the storage of failure data into the corresponding DRAM is finished, turning on a read/write operation flag and outputting a read/write trigger signal to start a read/write mode of operation of the DRAM when a refresh operation flag is turned off and the read/write request signal is supplied, a refresh trigger generator responsive to the refresh request signal for turning on the refresh operation flag and outputting a refresh start signal when the failure storage operation flag is turned off, a circuit for effecting operation modes of the DRAM, a timing generation memory for storing in advance timing data to refresh the DRAM and store the failure data into the DRAM, a program counter for generating address pointers for the timing generation memory, a sequence memory for storing sequence data to increment, decrement, and hold data in the program counter, the sequence memory having address pointers generated by the program counters, an operation mode register for storing start addresses of the timing generation memory and the sequence memory in each of the operation modes, and a sequence controller for operating the program counter according to the sequence data outputted from the sequence memory in response to the read/write trigger signal outputted from the read/write trigger generator or the refresh start signal outputted from the refresh trigger generator. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the programmable timing capabilities of Sato into the failure data collection of Yasui. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by using a programming means to collect failure data of particular interest would reduce testing time since the most vulnerable cells may be tested first.

As per claims 2 and 3, Yasui substantially teaches, in view of above rejections, (Figure 7) that each storage area 2 has a memory cell array MCA in which memory cells have been arrayed in a matrix manner of rows and columns, and in addition to the memory cell array MCA, is provided with a desired number of row spare lines SR and a desired number of column spare lines SC formed in the row address direction ROW and in the column address direction COL along the periphery of the memory cell array MCA, respectively. These spare lines SR and SC are provided for the purpose of relieving failure memory cells, and serve to change a memory under test that has been determined to be a defective or failure article to a non-defective or pass article by electrically replacing the detected failure memory cells in the storage area 2 with those spare lines. Further, in this example, a case is shown where two row spare lines SR are disposed along one side of the row address direction of the memory cell array MCA and two column spare lines SC are disposed along one side of the column address direction of the memory cell array MCA, respectively. The number of failure memory cells that can be relieved by the spare lines orthogonal to address line directions in the storage area 2 is restricted by the number of the spare lines SR formed in the row address direction ROW and the number of spare lines SC formed in the column address direction COL. For this reason, after the test is completed, at first the number of failure memory cells is obtained for each storage area 2, and row address lines and column address lines on which these failure memory cells are present are located for each storage area 2 to determine whether or not those failure memory cells on those address lines can be relieved by the spare lines orthogonal to their respective address lines.

As per claims 4-7, Sato substantially teaches, in view of above rejections, (col.7, lines 5-68) the memory controllers comprises a refresh timer for generating a refresh request signal, a failure storage trigger generator for being supplied with the failure storage signal and a one-address storage signal which is outputted each time the storage of failure data into the corresponding DRAM is finished, turning on a failure storage operation flag and outputting a failure storage trigger signal to start storing the failure data from the buffer memory means into the DRAM when a refresh operation flag is turned off and a count of the failure storage signal and a count of the one-address storage signal disagree with each other, a refresh trigger generator responsive to the refresh request signal for turning on the refresh operation flag and outputting a refresh start signal when the failure storage operation flag is turned off, a read/modify/write circuit for effecting the read/modify/write mode to store failure data into the DRAM, a timing generation memory for storing in advance timing data to refresh the DRAM and store the failure data into the DRAM, a program counter for generating address pointers for the timing generation memory, a sequence memory for storing sequence data to increment, decrement, and hold data in the program counter, the sequence memory having address pointers generated by the program counters, and a sequence controller for operating the program counter according to the sequence data outputted from the sequence memory in response to the failure storage trigger signal outputted from the failure storage trigger generator or the refresh start signal outputted from the refresh trigger generator.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
September 8, 2005

ALBERT DECADY
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